REMARKS

The comments of the applicant below are each preceded by related comments of the examiner (in small, bold type).

Non-Compliant Amendment Warning

4. Claim 15 is objected to because of the following informalities: Please correct line 5 from
"restore at two or more of the registers" to read --restore [[at]]two or more of the registers-Appropriate correction is required

Claim 15 has been amended.

6. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas, Jr., U.S. Patent Number 5,535,346 (herein referred to as Thomas).

7. Referring to claim 1, Thomas has taught a method comprising in a processor which has a future file (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51 ; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7) and which is capable of restoring two or more registers of the future file in a single clock cycle (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51 ; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7). Thomas has not explicitly taught restoring two or more registers of the future file over more than one clock cycle when a termination occurs in the processor. However, Thomas has disclosed in column 2, lines 12-19 a future file that "requires numerous cycles to correct its data in the event of an exception" but has a faster lookup for operand data and a future file that "requires only one cycle to correct the data stored in the future file in the event of an exception" but has a slower lookup for operand data. This would have suggested to a person of ordinary skill in the art to create a future tile that incorporates both advantages Then the device would benefit from both advantages dependent on the condition of the system. The future file would have faster exception handling and slower look-ups for data operands when there is a higher chance of an exception and fewer look-ups, but would have
faster look-ups for data operands and slower exception handling when there is more look-ups and lower chance of an exception.

The applicant respectfully disagrees. Although Thomas's background discloses two future file designs, one that restores the future file in one clock cycle and one that requires many, Thomas's subsequent focus is only on a future file that "can correct all of its data in a single cycle in the event of an instruction exception." (col. 7, ll. 36-38) It makes no mention of, in that same future file, restoring its data in more than one clock cycle. The only mention of restoring a

future file in more than one cycle is the mention in the background that there exist future files that "require[] numerous cycles." (col. 2, ll. 14, emphasis added) Thomas does not describe and would not have made obvious "restoring two or more registers of the future file over more than one clock cycle" in a processor "capable of restoring two or more registers of the future file in a single clock cycle."

The mere identification, that in the prior art, two known schemes have offsetting advantages and disadvantages is by no means a suggestion to combine them, as such a suggestion must include the suggestion that such a combination will work. Furthermore, the explicit statement that two competing schemes exist suggests that merely combining them is not possible, or at least not trivial, for if it were, there would be no need to identify the competing schemes as "compromises." (col. 2, ll. 10-11) There is no indication in Thomas that it is even possible to combine the two future file types mentioned in the background, no indication of how such a combination would be accomplished, and no indication that such a combination would somehow achieve both advantages while losing both disadvantages. The coincidence that Thomas talks about both schemes, and never mentions combining them, shows that the combination was not obvious.

10. Referring to claim 7, ...
13. Referring to claim 15, ...

Claims 7 and 15 are patentable for at least similar reasons as claim 1.

8. Referring to claim 2, ...
9. Referring to claim 3, ...
12. Referring to claim 8, ...
15. Referring to claims 4, 9, and 16, ...
16. Referring to claims 5, 10, and 17, ...
17. Referring to claims 6, 12, and 19, ...
18. Referring to claims 11 and 18, ...
19. Referring to claims 13 and 20, ...
20. Referring to claims 14 and 21, ...

The dependent claims are patentable for at least the same reasons as the claims on which they depend.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

No fees are believed due at this time. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 1/30/6

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